## IN THE CLAIMS

Please amend the claims as follows:

1.-11. (Cancelled).

12. (New) A multiple dispatch processor comprising:

a plurality of instruction fetch units, each instruction fetch unit capable of fetching a stream of instructions;

a plurality of instruction decode and dispatch units each coupled to a corresponding instruction fetch unit of the plurality of instruction fetch units to receive instructions therefrom;

at least one register file coupled for storing operands;

a plurality of execution units coupled to the register file and to the instruction decode and dispatch units for performing operations on operands as directed by the plurality of instruction decode and dispatch units; and

a resource allocation unit coupled to allocate execution units among the instruction decode and dispatch units; and

wherein the plurality of execution units further comprises a plurality of multifunction execution units, each of the multifunction execution units capable of handling integer and address operations.

13. (New) The multiple dispatch processor of Claim 12, wherein the plurality of execution units further comprises a plurality of floating point execution units.

14. (New) A multiple dispatch processor comprising:

a plurality of instruction fetch units, each instruction fetch unit capable of fetching a stream of instructions;

a plurality of instruction decode and dispatch units each coupled to a corresponding instruction fetch unit of the plurality of instruction fetch units to receive instructions therefrom;

at least one register file coupled for storing operands;

a plurality of execution units coupled to the register file and to the instruction decode and dispatch units for performing operations on operands as directed by the plurality of instruction decode and dispatch units; and

a resource allocation unit coupled to allocate execution units among the instruction decode and dispatch units;

wherein at least a first execution unit has a clock signal turned off when the first execution unit is marked unavailable in the resource available register, and the clock signal is turned on when the first execution unit is marked available in the resource allocation register.

15. (New) The multiple-dispatch processor of claim 14 wherein at least one execution unit is marked unavailable in the resource allocation register when the processor is operating under low power availability.

16. (New) The multiple-dispatch processor of claim 14 wherein the execution units further comprise a plurality of address-and-integer units and a plurality of floating point units.